CLAIMS

WE CLAIM:

1. A battery backed memory system comprising:

a first line receiving a source of line voltage;

volatile solid state memory storing data while receiving a voltage above a critical voltage level;

a second line receiving a source of battery voltage and providing the battery voltage to the volatile memory during a loss of line voltage;

a voltage sensor measuring the backup voltage relative to the critical voltage level and providing a signal; and

a microprocessor communicating with the volatile solid state memory and the voltage sensor and executing a program to determine whether the backup voltage was at or below the critical voltage level at any time during the loss of line voltage.

2. The battery backed memory system as recited in claim 1, further comprising nonvolatile solid state memory communicating with the microprocessor, wherein the program is read by the microprocessor from the nonvolatile memory.

3. The battery backed memory system as recited in claim 1, wherein the voltage sensor further comprises a supervisory circuit that measures voltage from the second line and outputs a signal comparing the measured voltage and an internal reference providing the critical voltage level.

4. The battery backed memory system as recited in claim 3, wherein the voltage sensor further includes a latch set by the signal from the supervisory circuit

5. The battery backed memory system as recited in claim 4 wherein the latch further communicates with the microprocessor to receive a signal indicating data in the volatile memory has been restored and resetting the latch.

6. The battery backed memory system as recited in claim 5, further comprising a switch that is controlled by the latch output and that, in turn, provides an input to the microprocessor while maintaining a high impedance between the latch and microprocessor.

7. The battery backed memory system as recited in claim 6, wherein the latch receives power from the second line.

8. The battery backed memory system as recited in claim 6, wherein the supervisory circuit receives power from the second line.

9. The battery backed memory system of claim 1 wherein the volatile memory includes memory selected from the group consisting of static and dynamic random access memory.

10. The battery backed memory system of claim 9 further including a DC/DC converter and wherein the volatile memory receives voltage from the second line via the DC/DC converter.

11. The battery backed memory system of claim 9 further including a voltage regulator circuit and wherein the volatile memory receives voltage from the second line via the voltage regulator circuit.

12. A method of controlling a battery backed memory system including a first line receiving a source of line voltage, volatile solid state memory storing data while receiving a voltage above a critical voltage level, a second line receiving a source of battery voltage to provide backup voltage to the volatile memory during a loss of line voltage, providing a signal measuring the backup voltage relative to the critical voltage level, and a microprocessor communicating with the volatile solid state memory and the voltage sensor, the method comprising the step of:

executing a program on the microprocessor that determines, based on the signal from the voltage sensor, whether the backup voltage was above the critical voltage level during the entire loss of line voltage.

13. The method as recited in claim 12, wherein the voltage sensor includes a supervisory circuit, the method further comprising the steps of:

measuring the voltage to the volatile memory at the supervisory circuit; and

outputting a signal comparing the measured voltage and an internal reference providing the critical voltage level.

14. The method as recited in claim 13, wherein the voltage sensor further includes a latch, the method further comprising the step of:

latching the output from the supervisory circuit.

15. The method of claim 14, wherein the battery-backed memory system further includes a switch that receives the latch output and communicates with a microprocessor input to provide a high impedance path there between.

16. The method as recited in claim 15, further comprising the step of resetting the latch after the determination by the microprocessor whether the backup voltage was above the critical voltage level during the entire loss of line voltage.

17. A method of verifying a status of battery-backed volatile memory that requires a critical voltage level to maintain integrity of data stored therein, the steps comprising:

(A) providing voltage from a primary source to the volatile memory at a level greater than the critical voltage level;

(B) providing the volatile memory with backup voltage from a backup source during an interruption of the primary source;

(C) measuring the backup voltage during the interruption; and

(D) outputting a signal indicating that whether the backup voltage was above the critical voltage level during the entire interruption.

18. The method as recited in claim 17, further comprising, after step (D):

(E) restoring the voltage from the primary source to the volatile memory; and

(F) executing a program at a microprocessor to determine, based on the signal, whether data integrity was maintained in the volatile memory during the interruption.

19. The method as recited in claim 18, further comprising loading the data from volatile memory to execute a control function at the microprocessor if data integrity was maintained.

20. The method as recited in claim 18, further comprising determining that an error condition exists if the backup voltage was not maintained above the critical voltage level during the interruption.